

# **A Design of 8-bit Pipelined ADC for High Speed Applications Using Cadence Virtuoso**

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**ABSTRACT:** - Nowadays, several applications insist to have high performance data converters. These data converters should have gainful specifications of sampling rate, resolution and less power dissipation. These are the necessary ADC requirements for the wireless communication applications, Broadband transceivers and also for countless digital devices. This project is dedicated to the development of Pipeline Architecture ADC with less power dissipation, high resolution and high speed. In this project, an 8-bit ADC with 1-bit resolution to each stage is designed by Cadence virtuoso software tool with 180nm technology. The main block for pipeline architecture is an operational amplifier. Pipeline architecture and Opamp works with 1.8V supply voltage.

**KEYWORDS:** ADC, VLSI, INL, DNL, Opamp.

## **I. INTRODUCTION**

Analog to Digital Converters (ADC) are basic building blocks for mixed and analog signal processing. ADCs will link the natural world (analog signals) and the digital world (digital signal). An extensive implementation of digital computation and signal processing used in communications, instrumentation, industrial control, and image processing and digital to analog and analog to digital conversion applications in a field is expanding tremendously. In this modern era, the electronic systems are influenced by digitization. Everywhere digital circuits and digital processing are used. The development of digital integrated circuits is promoted by synthesis tools and computer-aided design (CAD) analysis. Although digital circuits are gradually replacing an analog circuit, but our world is analog in nature. The signals which appear in nature are always analog, such as voltage, current, speed, temperature, pressure, time, voice, etc. And also the human perception and storage of information is the analog mode. The main reason for the digitization of electronic systems is low noise sensitivity, high stability, strong anti interference and wide adaptability. And digital circuits also have features like easy to design, more extensive programmability and automated testing. New generation of digital circuits uses Large-scale integration (VLSI) technology to achieve lower power consumption, higher speed, more features per chip, and cost. Analog to Digital Converter is the device which converts analog input signal into digital values.

## **II. PIPELINE ANALOG-TO-DIGITAL CONVERTER**

Pipelined Analog-to-Digital Converter is an architecture which offers the attractive combination of low power dissipation, high resolution and high speed. Hence the Pipelined ADC is an optimum solution for low power applications like wireless communication systems.

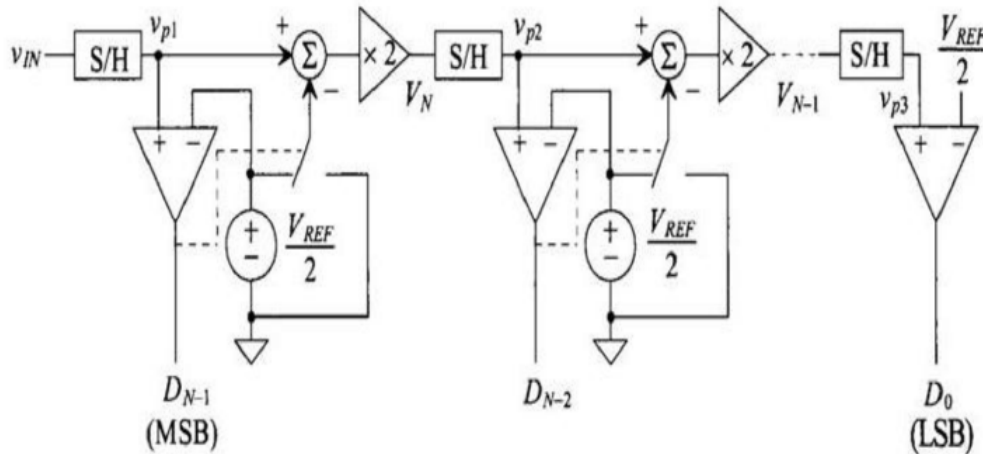


Figure 1 Pipeline Architecture

The CMOS IC technology is widely for digital and analog applications. Pipeline architecture allows digital gain calibration, power minimization and also digital error correction through capacitor scaling. Hence, for high resolution and high speed application Pipeline ADC is suitable.

#### A. DESIGN OF AN OPERATIONAL AMPLIFIER

To design a Pipelined ADC the basic block is Operational Amplifier. Opamp is designed using gpdk 180nm technology with 1.8V power supply. Before starting the design, there are many specifications that need to be assumed or taken into consideration. Design specifications for an operational amplifier are mentioned below:

Table 1: Design specifications

Parameter	Values
DC Gain	1000=60 DB
Phase margin	=>60°
Slew rate	20V/ μ.sec
ICMR	0.8V to 1.6V
CL	2pF
VDD	1.8V

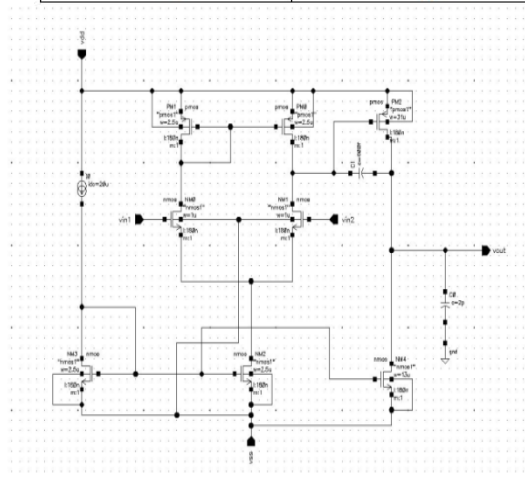


Figure 2: Opamp Circuit

**III. THE SUB-BLOCKS OF PIPELINE ARCHITECTURE**

Pipeline architecture consists of sample and hold, subtractor, comparator, transmission gate switch and also residue amplifier. Each block will be explained below.

**A. LATCH COMPARATOR**

Compare to normal comparator, latch comparator is better because overall power dissipation of the 8-bit pipeline architecture can be reduced. The schematic diagram for the latch comparator is shown in figure 3. Latch comparator will compare an input signals only at the rising edge of the latch signal. “AND” circuit is also needed to implement this comparator and layout for “AND” will be shown below.



Figure 3 :(a) Latch Comparator, (b) NAND Gate Circuit

**B. SAMPLE AND HOLD CIRCUIT**

The schematic of sample and hold circuit has been displayed in figure 4. An operational amplifier will act as a voltage follower circuit. The use of voltage follower is to eliminate impedance mismatch.

**C. SUBTRACTOR**

In pipeline architecture subtractor circuit is used to subtract the sample and hold’s output and transmission gate switch output. And output of subtractor is given to the residue amplifier. To understand the operation subtractor circuit is displayed in figure 4.

**D. RESIDUE AMPLIFIER**

The residue amplifier is used to increase the gain of the degraded signal. Circuit for residue amplifier which is generated using Opamp circuit and it is shown in figure 5.

**E. TRANSMISSION SWITCH**

Transmission gate is been used in 8-bit pipeline architecture and gate can be constructed by using two inverters. Output of the latch comparator is the select line for the comparator and output of the gate is the input to an inverting terminal of subtractor circuit. Circuit and layout is shown in below.

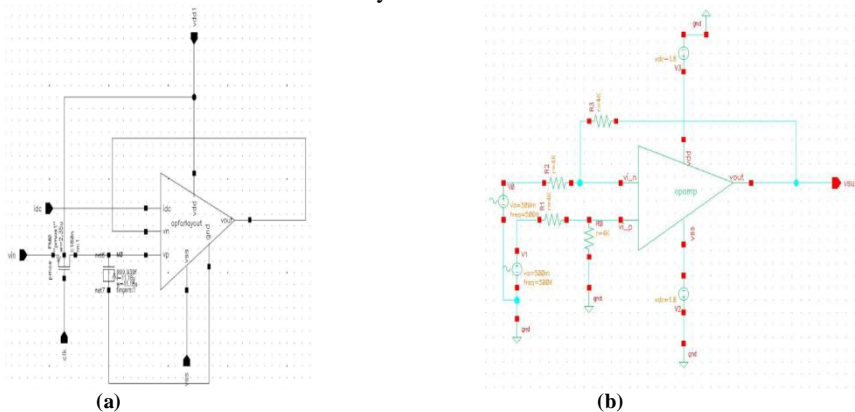


Figure 4: (a) Sample & Hold circuit (b) Subtractor circuit

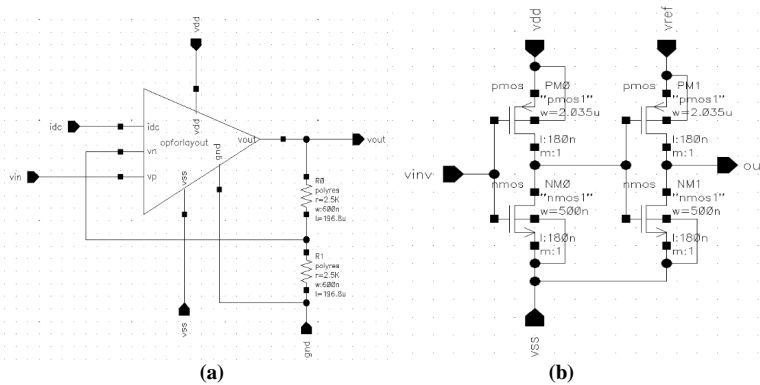


Figure 5: (a) Residue amplifier circuit (b) Transmission switch

**F. FIRST STAGE OF PIPELINE ARCHITECTURE**

First stage consists of sample and hold, subtractor, comparator, transmission gate switch and also residue amplifier. First stage is depicted in figure g. Layout structure for the one stage of the pipeline architecture is displayed in figure 6.

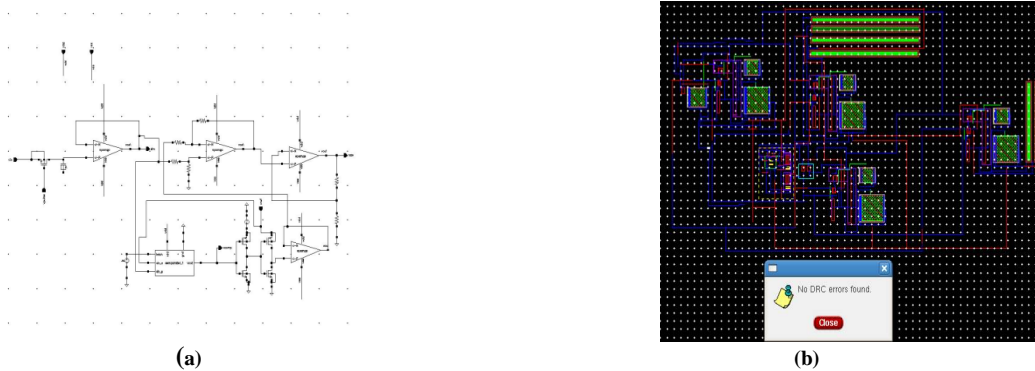


Figure 6: (a) Circuit for first stage (b) Layout for one stage

**G. 8-BIT PIPELINE ARCHITECTURE**

Figure 7 displays the 8 stages of the pipelined architecture. Each stage is cascaded, eight output bits are obtained.

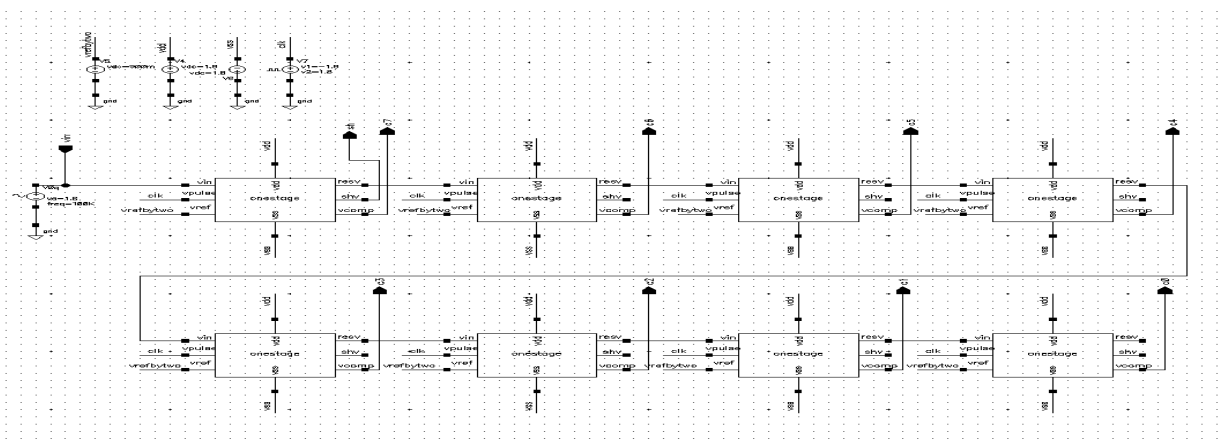
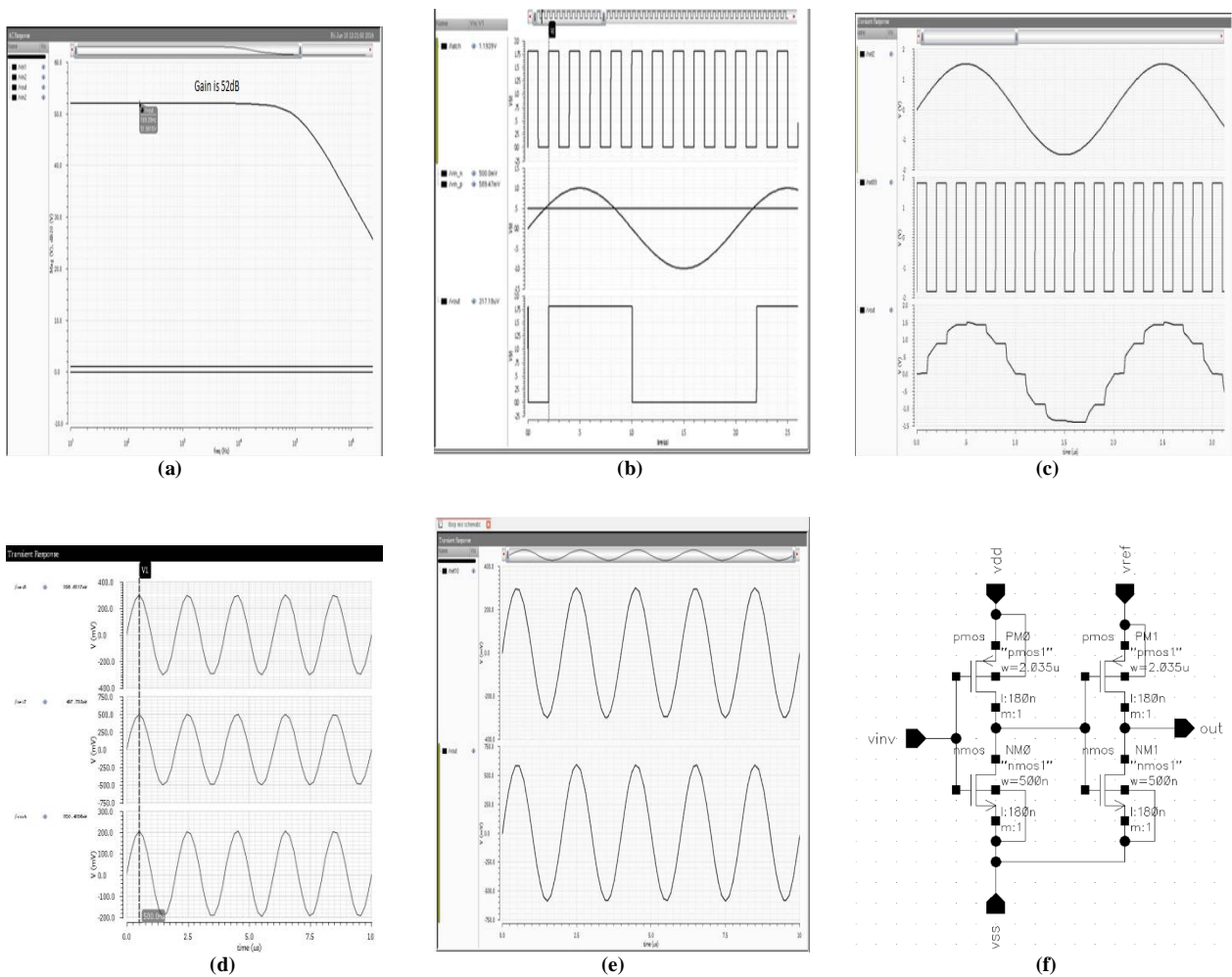


Figure 7 8-stage Pipeline ADC

## IV. SIMULATION AND RESULT ANALYSIS

Simulation results for all sub-blocks are shown below. To obtain the gain of an Opamp, AC analysis on the Opamp schematic is done. Frequency range 10 – 100MHz is given, the gain obtained is 52dB. Opamp gain is shown in figure 8. The output of latch comparator, sample and hold circuit, subtractor, residue amplifier transmission switch is shown in figures b, c, d, e f, respectively.



**Figure 8:** (a) OPAMP Gain, (b) Waveform for latch comparator circuit, (c) Waveform for Sample & Hold, (d) Waveform for Subtractor, (e) Waveform for Residue Amplifier, (f) Waveform for Transmission Switch

Waveforms for 8-stages pipeline ADC is depicted below. When an input is 1.8V, reference voltage (Vref) is 2.2V and expected code is 11010001 and waveform for this input value is shown in 9. Power dissipation is 28.mW.

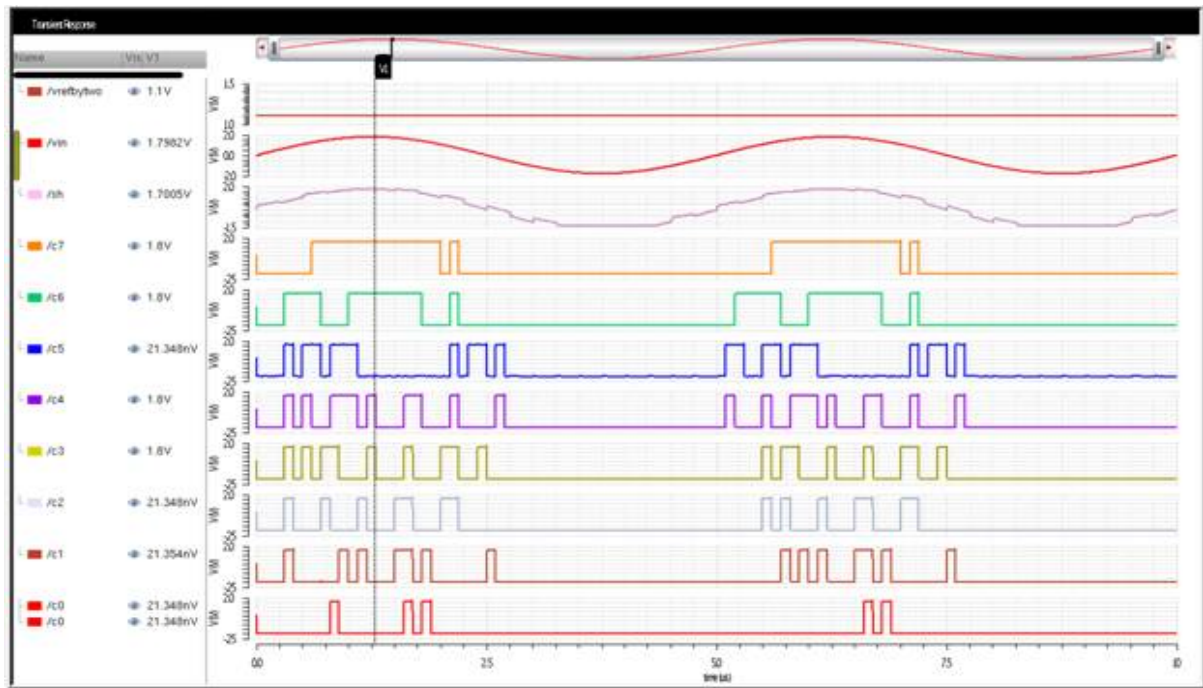


Figure 9 Waveform for 8-bit ADC

#### IV. CONCLUSION

The Pipeline Architecture has been implemented by using the sub-blocks like latch comparator, Subtractor, Sample and Hold Circuit and Residue Amplifier. The main aim was to reduce the power dissipation and width as much as possible. Power dissipation obtained for this 8-bit architecture is 28mW and Layout for all sub-blocks and for one stage pipeline ADC with DRC and LVS checks has been implemented

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